diffuses less, and therefore the difference in diffusion profile is minimized. However, the restriction of high temperature processes, referred to as the "thermal budget", places significant constraints on the ability to fabricate the remainder of the integrated circuit in the optimal manner. In addition, this differential diffusion has also required separate emitter anneals to be performed for the NPN and PNP devices, with one anneal (typically an RTA) performed after the formation of one emitter electrode type and before the formation of the other, followed by a second RTA received by both device types. However, this approach drives up manufacturing costs, and results in tradeoffs between complementary emitter matching and other device parameters.

BRIEF SUMMARY OF THE INVENTION

[0012] It is therefore an object of the present invention to provide a method of fabricating a bipolar integrated circuit, and an integrated circuit device so fabricated, in which the diffusion of emitter dopant can be readily controlled.

[0013] It is a further object of this invention to provide such a method and device in which the diffusion of both conductivity types of dopant can be controlled to more closely match one another.

[0014] It is a further object of this invention to provide such a method and device in which constraints on the thermal budget for processes after formation of the emitter are relaxed.

[0015] It is a further object of this invention to provide such a method and device which is also compatible with the formation of MOS transistors in the same integrated circuit.

[0016] It is a further object of this invention to provide such a method and device in which the emitter resistance is reduced by the removal of native oxides at the emitter-base interface.

[0017] Other objects and advantages of the present invention will be apparent to those of ordinary skill in the art having reference to the following specification together with its drawings.

[0018] The present invention may be implemented by doping the emitter polysilicon electrodes with their corresponding emitter dopant in combination with a diffusion retardant, such as a carbon-bearing species or nitrogen. The retardant slows the diffusion rate of boron and of many n-type dopants, reducing the sensitivity of the emitter diffusion to time and temperature and thereby relaxing the thermal budget of subsequent processes. This effect improves the matching of complementary bipolar transistors with one another, and is compatible with the formation of MOS transistors in the same device.

[0019] According to another aspect of the invention, the carbon-bearing species both retards the diffusion of boron (p-type dopant) and enhances the diffusion of arsenic (n-type dopant), which otherwise diffuses more slowly than boron. Closely-matched emitters are formed from boron-doped and arsenic-doped polysilicon emitters that are doped with a carbon-bearing species.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0020] FIGS. 1*a* and 1*b* are cross-sectional views of a conventional bipolar transistor.

[0021] FIGS. 2*a* through 2*f* are cross-sectional views of bipolar transistors constructed according to the preferred embodiments of the invention.

[0022] FIG. 3 is a cross-sectional view of a metal-oxide-semiconductor (MOS) transistor constructed according to the preferred embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0023] The present invention will now be described in connection with its preferred embodiments. These exemplary embodiments are directed to the fabrication of bipolar junction transistors in a silicon-on-insulator (SOI) structure. It will be appreciated by those skilled in the art having reference to this specification that the present invention may be used to form either PNP or NPN transistors, or both as may be used in a complementary bipolar or BiCMOS technology, as well as used to form other alternative structures. In addition, while this invention is particularly beneficial as applied to SOI structures, it is also contemplated that this invention may also be utilized in bulk integrated circuit devices, where no buried insulator layer is present. Furthermore, while these embodiments are silicon or SiGe NPN and PNP bipolar transistors, it is contemplated that the present invention will be equally applicable to emerging bipolar technologies such as SiGeC (silicon-germanium-carbon) and SiC bipolar technologies It is therefore to be understood that these and other alternatives to the embodiments described below are contemplated to be within the scope of the invention as claimed.

[0024] Referring now to FIGS. 2*a* through 2*f*, the construction of complementary bipolar transistors 20*p*, 20*n* according to the preferred embodiments of the invention will now be described, by way of example. In this example, transistor 20*p* is a PNP bipolar transistor, while transistor 20*n* is an NPN bipolar transistor. As will be described in further detail below, it is contemplated that the method according to these embodiments of the invention can also be applied to the manufacture of integrated circuits that include both bipolar and MOS transistors, and indeed that include bipolar and MOS transistors of both conductivity types, according to a CBiCMOS technology. Those skilled in the art will also recognize, based on this specification, that other active and passive components may also be fabricated, on the same integrated circuit, as transistors 20*p*, 20*n*.

[0025] FIG. 2*a* illustrates a partially-fabricated integrated circuit wafer at which transistors 20 are to be fabricated. Of course, at the point in the process flow illustrated in FIG. 2*a*, transistors 20*p*, 20*n* are not yet formed (i.e., necessary elements such as an emitter are not yet present), and as such reference numerals 20*p*, 20*n* refer to the locations at which transistors 20*p*, 20*n* will be formed.

[0026] Referring first to FIG. 2*a*, the construction of PNP transistor 20*p* according to the preferred embodiment of the invention will now be described in detail. The cross-section of FIG. 2*a* illustrates buried insulator layer 24 in place over substrate, or handle wafer, 22 in the typical manner for silicon-on-insulator (SOI) structures. Buried insulator layer 24 is typically silicon dioxide, and as such is generally referred to as buried oxide. A single-crystal silicon thin film layer including buried collector layers 26*p*, 26*n* is disposed over buried oxide layer 24. The formation of the structure of